proposed drawing change in red. Applicants respectfully request that the proposed drawing change be approved and entered in the application.

The specification was objected to because on page 8, line 12, reference number "84" should be 83. Applicants have corrected the specification as set forth above.

Claims 2-4 and 7 were rejected under 35 U.S.C. § 112, second paragraph, as indefinite. Applicants have amended claims 2-4 and 7 to overcome the indefiniteness identified by the Examiner in each of these claims.

Turning to the merits, claims 1, 2, 11, and 15 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 5,856,702 ("Hashimoto"). Claims 1, 7, 8, and 10 were rejected under 35 U.S.C. § 102(e) as anticipated by or in the alternative under 35 U.S.C. § 103(a) as obvious over Hashimoto. Claims 1, 3, and 4 were rejected under 35 U.S.C. § 103(a) as obvious over Hashimoto in view of U.S. Patent No. 5,753,391 ("Stone et al."). Claims 11 and 16 were rejected under 35 U.S.C. § 103(a) as unpatentable over Hashimoto in view of U.S. Patent No. 6,054,359 ("Tsui et al.").

Applicants respectfully disagree with the bases for the rejections and request reconsideration and further examination of the claims.

The disclosed and claimed embodiments of the invention are directed to a resistive structure having a high layer resistance value and, more particularly, is configured to tolerate high voltage values without necessarily employing cumbersome structures. As a resistor element, a polysilicon filling is placed in a trench that has previously been oxidized according to known methods. The polysilicon is then doped by implantation to be used as a resistive element. The oxide layer around the filing polysilicon not only dielectrically isolates the resistor from the other components, but it also gives the structure a good voltage capacity and, as it is clearly shown in the description, is suitable for all uses in which high voltage supply is required. To achieve the foregoing, the dielectric trench is formed to have a depth greater than a width. In addition, in one embodiment the width of the dielectric increases along the resistor length in which the voltage drop increases. This provides increased insulation where there is a greater voltage drop.

Not disclosed (actually comparison between 3 & 4 in fig 6)

Hashimoto, U.S. Patent No. 5,856,702, teaches, in its main embodiment in Figures 2 and 3, a doped polysilicon resistive structure deposited according to slots that are previously produced on a dielectric layer. The dielectric layer has an even thickness across the

entire wafer surface and is considered to be a surface layer, which is one of those layers usually used to isolate silicon surfaces (as for instance a thick oxide layer defining an active area). Hashimoto's purpose is to obtain a surface resistive structure dielectrically isolated to guarantee a minor integration area (with respect to conventional polysilicon surface resistors, the reduction of the area is of about 16%). Clearly Hashimoto does not teach a trench having a depth greater than a width. Rather, in Hashimoto the dielectric layer is a planar structure having a width greater than a depth across the entire wafer, and the polysilicon layer forming the resistor is integrated on this dielectric layer (previously etched so as to create some slots). Thus, in Hashimoto the objective is to limit the thickness of the dielectric layer whereas in the present invention the trench and the resistive structure do not have an intrinsic limit with respect to the depth parameter. Moreover, nowhere does Hashimoto teach or suggest the trench formed to have a widening dielectric region along the trench so that the obtained resistance can tolerate a high voltage supply where the voltage drop increases.

Stone, U.S. Patent No. 5,753,391, discloses a resistor having a serpentine layout. The resistor structure and its operation are clearly different from that of the present invention, and this reference is cited only to show the serpentine shape.

yet amended the claim as a serpentine

Tsui et al., U.S. Patent No. 6,054,359, teaches a resistor produced by two polysilicon layers, one of which is doped so as to obtain high values in the layer. Nowhere does Tsui et al. teach or suggest forming a resistive structure by using a trench or similar process. It appears this reference has been cited only because of its teachings with respect to doping techniques.

Turning to the claims, claim 1 is directed to a resistive structure integrated in a semiconductor substrate that comprises a trench having a depth greater than a width and lined with dielectric material to form a dielectric trench; and a polysilicon region, at least a portion of which is doped, completely surrounded by the dielectric trench so that the resistive structure is isolated electrically from other components jointly integrated in the semiconductor substrate. As discussed above, nowhere does Hashimoto teach or suggest a trench having a depth greater than a width to form a dielectric trench that is filled with a polysilicon region, at least a portion of which is doped, so that the resistive structure is isolated electrically from other components jointly integrated in the semiconductor substrate. There is neither any suggestion nor any teaching in Hashimoto or Stone, taken alone or in any combination thereof, with respect to the

combination recited in claim 1, as discussed above. If one were motivated to combine the references as suggested by the Examiner, the resulting structure would fail to meet the limitation of claim 1, in part because its depth would be much less than its width.

Claim 2, which depends from claim 1, further recites the dielectric trench formed with a plurality of trenches distributed about the polysilicon region to form a single dielectric region having a width that increases along the resistive structure in which a voltage drop increases. This is the embodiment shown in Figure 7 wherein the width of the dielectric portion increases along the length of the resistive structure to provide increasing insulation where the voltage drop increases. There is no teaching or suggestion in Hashimoto of such a structure.

Claim 3, which depends from claim 1, recites the polysilicon region and the dielectric region having a serpentine pattern to reduce the space requirements of the resistive structure. Claim 4, which depends from claim 3, recites the serpentine pattern to be formed of rungs that are physically connected and paralleled together by metalization. Applicants respectfully submit that claim 1 and dependent claims 2-4, 7, 8, and 10 are all allowable over the references cited by the Examiner.

Claim 11 is directed to an integrated resistive structure that comprises at least one trench having at least one trench having a depth greater than a width formed in a semiconductor substrate; a dielectric layer entirely coating all walls of the at least one trench; and a polysilicon region filling the at least one trench to be isolated dielectrically from the semiconductor substrate, the polysilicon region having at least a portion that is doped. As discussed above with respect to claim 1, no where does Hashimoto teach or suggest a trench having a depth greater than a width that is coated by a dielectric layer. Applicants submit that claim 11 is allowable over Hashimoto.

Claims 15, 16, and all depend from claim 11, and applicants submit that these claims are allowable for the reasons why claim 11 is allowable.

New claim 19 is in essence claims 1 and 2 combined together. New claim 20 is a combination of claims 1, 2, and 7. Applicants respectfully submit that claims 19 and 20 are allowable for the reasons why claim 2 and claim 7 are allowable.

The Commissioner is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

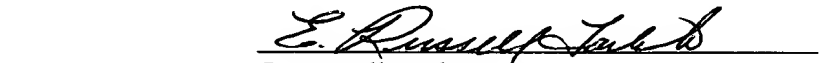
Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version With Markings to Show Changes Made.**"

In view of the foregoing, applicants respectfully submit that all of the claims remaining in this application are now in condition for allowance. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicants' undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

Respectfully submitted,

Salvatore Leonardi et al.

SEED Intellectual Property Law Group PLLC



E. Russell Tarleton
Registration No. 31,800

ERT:aep

Enclosure:
Postcard
Request for Drawing Change
Redlined Figure 9
Formal Figure 9

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Paragraph beginning at page 8, line 12 has been amended as follows:

In the winding resistive structure 81, the dielectric region 84 also surrounds the polysilicon region 834 completely, both regions conforming to the winding shape of the resistive structure 81.

In the Claims:

Claims 1-4, 7, 10, and 11 have been amended and new claims 19 and 20 have been added as follows:

1. (Amended) A resistive structure, integrated in a semiconductor substrate, comprising: a trench having a depth greater than a width and lined with dielectric material to form a dielectric trench and a ~~suitably doped~~ polysilicon region, at least a portion of which is doped, the polysilicon region completely surrounded by ~~a~~ the dielectric ~~region~~ trench, so that the resistive structure is isolated electrically from other components jointly integrated in the semiconductor substrate.

2. (Amended) The resistive structure of claim 1, wherein portions of the ~~resistive structure~~ dielectric trench are formed with a plurality of trenches ~~having suitable areas and are~~ distributed about the polysilicon region to form a single dielectric region having a width that increases along the resistive structure in which a voltage drop increases.

3. (Amended) The resistive structure of claim 1, wherein said polysilicon region and said dielectric region ~~are winding patterns~~ have a serpentine pattern, thereby reducing the space requirements of the resistive structure for a given resistance value.

4. (Amended) The resistive structure of claim 3, wherein said ~~winding patterns~~ serpentine pattern is ~~are~~ formed to include rungs, said rungs are physically connected in parallel together by a metallization.

7. (Amended) The resistive structure of claim 1, wherein said polysilicon region comprises two deposited layers of ~~undoped~~ polysilicon, only a first of said layers being enhanced by implantation to lower the values of parasitic capacitances associated with the resistive structure.

10. (Amended) The resistive structure of claim 1, wherein said dielectric region that is arranged to isolate the resistive structure is formed in the process of oxidizing the sidewalls of ~~a~~ the dielectric trench.

11. (Amended) An integrated resistive structure, comprising:

at least one trench having ~~sidewalls~~ a depth greater than a width formed in a semiconductor substrate;

a dielectric layer entirely coating all walls of the at least one trench; and

a polysilicon region filling the at least one trench to be isolated dielectrically from the semiconductor substrate, the polysilicon region having at least a portion that is doped.

19. (New) A resistive structure, integrated in a semiconductor substrate, comprising:

a trench having a depth greater than a width and lined with dielectric material to form a dielectric trench, the dielectric trench formed with a plurality of trenches distributed to form a single dielectric region having a width that increases along the resistive structure where a voltage drop increases; and

a polysilicon region, at least a portion of which is doped, filling the dielectric trench to be surrounded by the dielectric material.

20. (New) A resistive structure, integrated in a semiconductor substrate, comprising:

a trench having a depth greater than a width and aligned with dielectric material to form a dielectric trench, the dielectric trench formed with a plurality of trenches distributed to form a single dielectric region having a width that increases along the resistive structure where a voltage drop increases; and

a polysilicon region filling the dielectric trench to be surrounded by the dielectric material, the polysilicon region comprising two deposited layers of polysilicon, only a first of the layers enhanced by implantation to lower the values of parasitic capacitances associated with the resistive structure.

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